REMARKS

In the Office Action dated May 3, 2004, pending Claims 1-4 were rejected and the rejection made final. In response Applicant has filed herewith a Request for Continued Examination and has rewritten the pending claims. Applicants intend no change in the scope of the claims by the changes made by this amendment. It should be noted these amendments are not in acquiescence of the Office's position on allowability of the claims, but merely to expedite prosecution.

Applicant and the undersigned are most grateful for the time and effort accorded the instant application by the Examiner. On July 8, 2004, Applicant's counsel conducted a telephone interview with the Examiner during which the present application and the applied art were discussed. No agreement was reached with respect to the claims.

Claims 1-4 are pending in the application. Claims 1, 2, and 3 are independent claims; claim 4 is a dependent claim. All claims have been rejected under 35 U.S.C. § 103(a). Claim 1 stands rejected under 35 U.S.C. 103(a) over Upton in view of Figure 2 and statements made in the specification (pages 1-3) and further in view of "Official Notice". Claims 2-4 also stand rejected under 35 U.S.C. 103(a) over Upton in view of Figure 2 and statements made in the specification (pages 1-3). Reconsideration and withdrawal of the present rejections are hereby respectfully requested.

The present invention broadly contemplates a method and circuit in order to improve the usage of FPGAs during the use by end-users and during development of circuits implementing some new functionality on FPGAs. (Page 4, lines 2-3) Typically,

such FPGAs are disposed on a PCI Card within a personal computer. In accordance with the present invention, no access is needed to replace PROMs or to connect external equipment to the card which is used to reprogram EEPROMs. Programming and updating hardware electronic circuits is accomplished without manually accessing the circuits. (Page 4, lines 4-6) Since any manual access to PC-cards causes additional work and increases the risk of damage to other hardware connected in the casing of the computer, e.g., by statical charges brought to any of a plurality of locations sensitive thereto, the present invention decreases both the work necessary to reprogram FPGAs and the associated risk.

As set forth in the figures, the present invention is address the relationship between a PROM, an EEPROM, an FPGA and a MUX. Figure 1 is a schematic representation of a structural diagram of the essential elements of a circuit according to a preferred embodiment of the present invention. Figure 3 is schematic representation of a block diagram showing the essential steps of the method of the present invention. In summary, once the FPGA is configured for device level communications via the PROM, it is determined whether the FPGA is to be reconfigured. If yes, the EEPROM is programmed via an FPGA implemented function with the new configuration. Then, the FPGA is configured with the configuration contained in the EEPROM (either the original configuration or the new configuration).

The comments in the previous *Amendment* regarding Upton are equally applicable here. Upton as best understood appears to be directed to reconfigurable processors, that is, a processor whose architecture can be interchanged among classical Von Neumann

architecture and other architectures such as parallel, systolic, pipeline, etc., very quickly. (Col. 1, lines 12; Col. 3, lines 9-11) Each type of architecture appears to require different function sequences (120-1 through 120-N) which are stored in macro array library 204 with programmable read only memory modules (PROMs) 210, 212, 214 and 216 which store function sequences 120-1 through 120-N. Data link 300 appears to be used for "reconfiguring" the PROMs, i.e., making certain PROMs available and thereby making certain function sequences available, depending upon which type of architecture is being used.

The instantly claimed invention requires specifically "a MUX element, adapted such that the configuration data is capable of being read from the FPGA to the EEPROM" and "switching said MUX element such that the configuration data is capable of being read from said EEPROM into said FPGA". (Claim 1) Similar language appears in the other independent claims. At a minimum, the use of a switchable, bi-directional MUX element is simply not taught or suggested by Upton. Indeed, in Upton the data flow through the MUX is always from the a PROM to the PGA. (*See* Fig. 7)

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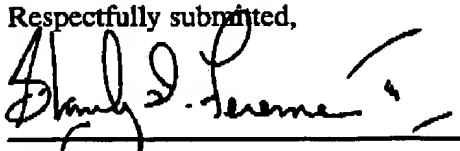
In view of the foregoing, it is respectfully submitted that Claims 1, 2, and 3 are fully distinguishable over the applied art and are thus allowable. By virtue of dependence from Claim 3, it is thus also submitted that Claim 4 is also allowable at this juncture. Notice to the effect is hereby earnestly solicited.

Respectfully submitted,



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